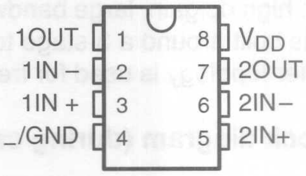
TLC4502, TLC4502A, TLC4502Y
Advanced LinEPIC™ SELF-CALIBRATING (Self-Cal™) PRECISION DUAL OPERATIONAL AMPLIFIERS

SLOS161A – OCTOBER 1996 – REVISED NOVEMBER 1996

- **Power On Calibration of Input Offset Voltage**
- **Low Input Offset Voltage . . . < 50 µV Max (TLC4502A)**
- **Low Input Offset Voltage Drift . . . < 1 µV/°C**
- **Low Input Bias Current**
- **High Output Drive Capability C_L < 1 nF and R_L > 1 kΩ**
- **High Open Loop Gain . . . > 120 dB**
- **Rail-To-Rail Output Voltage Swing**
- **Low Distortion . . . < 0.01% at 10 kHz**
- **Low Noise . . . 12 nV/√Hz at 1 kHz**
- **High Slew Rate . . . 2.5 V/µs**
- **Low Power Consumption . . . < 1.5 mA (Typical) Per Amplifier**
- **Short Calibration Time . . . 300 ms Typ**

D PACKAGE
(TOP VIEW)



description

The TLC4502 self-calibrating operational amplifier utilizes the recent availability of on-chip digital and analog signal processing to automatically null the input offset voltage at power-up. This *self-calibrating* feature requires typically 300 ms to complete and is repeatable to within ±3 µV on successive calibrations. The technique involves the extraction and digital storage of the key offset-nulling information. This information is retained without degradation as long as the circuit is powered. This eliminates the need for continuous chopping of the input signal to refresh the offset information. Once the process is complete, the bulk of the calibration circuitry drops out of the signal path and shuts down. This minimizes or eliminates any effect the calibration circuitry might have on the desired signal path. It also allows the TLC4502 to be used exactly like any other operational amplifier after the calibration cycle is complete.

The TLC4502 is a high-performance operational amplifier fabricated in a 1-µm 5-V digital CMOS technology. It achieves very high dc gain, as well as excellent power supply rejection ratio (PSRR) and common-mode rejection ratio (CMRR). It uses a mixed-mode (analog/digital) internal compensation loop with digital storage of the offset information and a current-mode output to reduce its input offset to < 50 µV. The TLC4502 also features a rail-to-rail output structure capable of driving loads to 1 kΩ and 1 nF. Unlike existing commercially available low-offset high-precision amplifiers, the TLC4502 needs only a single 5-V supply, requires no trimming, and uses no bipolar transistors or JFETs.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICE† SMALL OUTLINE (D)	CHIP FORM (Y)
0°C to 70°C	50 µV	TLC4502ACDR	TLC4502Y
	100 µV	TLC4502CDR	
–40°C to 85°C	50 µV	TLC4502AIDR	
	100 µV	TLC4502IDR	

† The D package is available taped and reeled.

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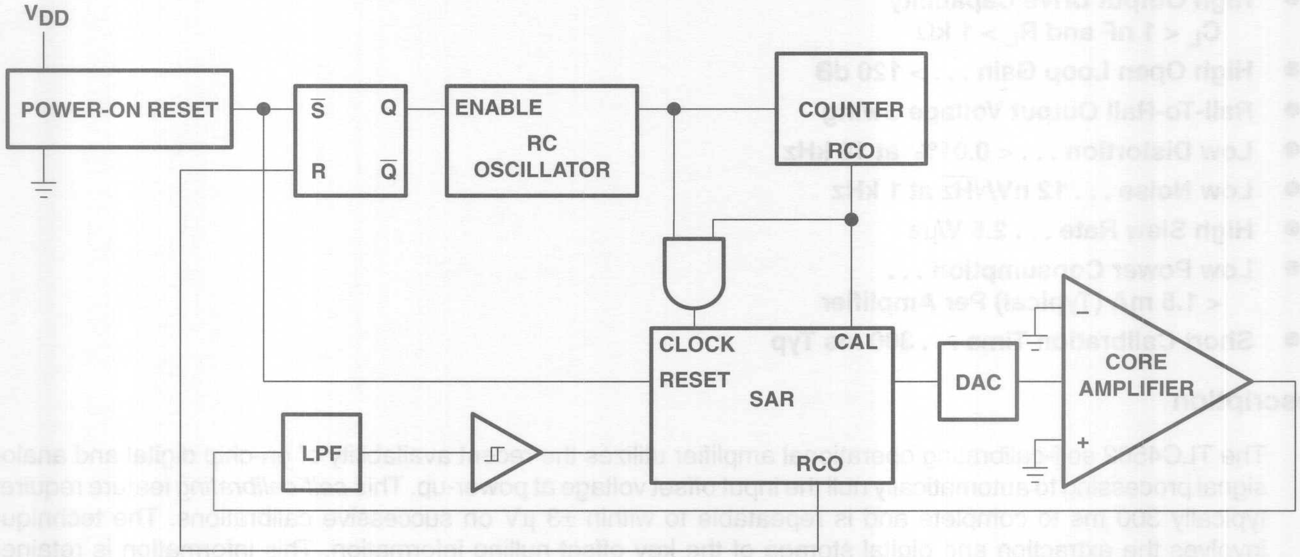
TEXAS INSTRUMENTS

description (continued)

To achieve high dc gain, large bandwidth, high CMRR and PSRR, as well as good output drive capability, the TLC4502 is built around a 3-stage topology: two gain stages, one rail-to-rail, and a class-AB output stage. A nested Miller topology is used for frequency compensation.

functional block diagram (during calibration)



During the calibration procedure, the operational amplifier is removed from the signal path and both inputs are tied to GND.

The class AB output stage features rail-to-rail voltage swing and incorporates additional switches to put the output node into a high-impedance mode during the calibration cycle. Small-replica output transistors (matched to the main output transistors) provide the amplifier output signal for the calibration circuit. The TLC4502 also features built-in output short-circuit protection. The output current flowing through the main output transistors is continuously being sensed. If the current through either of these transistors exceeds the preset limit (60 mA – 70 mA) for more than about 1 µs, the output transistors are shut down to essentially their quiescent operating point for approximately 5 ms. The device is then returned to normal operation. If the short circuit is still in place, it is detected in less than 1 µs and the device is shutdown for another 5 ms.

The offset cancellation uses a current-mode digital-to-analog converter (DAC), whose full-scale current allows for an adjustment of approximately ±5 mV to the input offset voltage. The digital code producing the cancellation current is stored in the successive-approximation register (SAR).

During power up, when the offset cancellation procedure is initiated, an on-chip RC oscillator is activated to provide the timing of the successive-approximation algorithm. To prevent wide-band noise from interfering with the calibration procedure, an analog low-pass filter followed by a Schmidt trigger is used in the decision chain to implement an averaging process. Once the calibration procedure is complete, the RC oscillator is deactivated to reduce supply current and the associated noise.

The key operational-amplifier parameters CMRR, PSRR, and offset drift were optimized to achieve superior offset performance. The TLC4502 calibration DAC is implemented by a binary-weighted current array using a pseudo-R-2R MOSFET ladder architecture, which minimizes the silicon area required for the calibration circuitry, and thereby reduces the cost of the TLC4502.

description (continued)

Due to the performance (precision, PSRR, CMRR, gain, output drive, and ac performance) of the TL
is ideal for applications like:

- Data acquisition systems
- Medical equipment
- Portable digital scales
- Strain gauges
- Automotive sensors
- Digital audio circuits
- Industrial control applications

It is also ideal in circuits like:

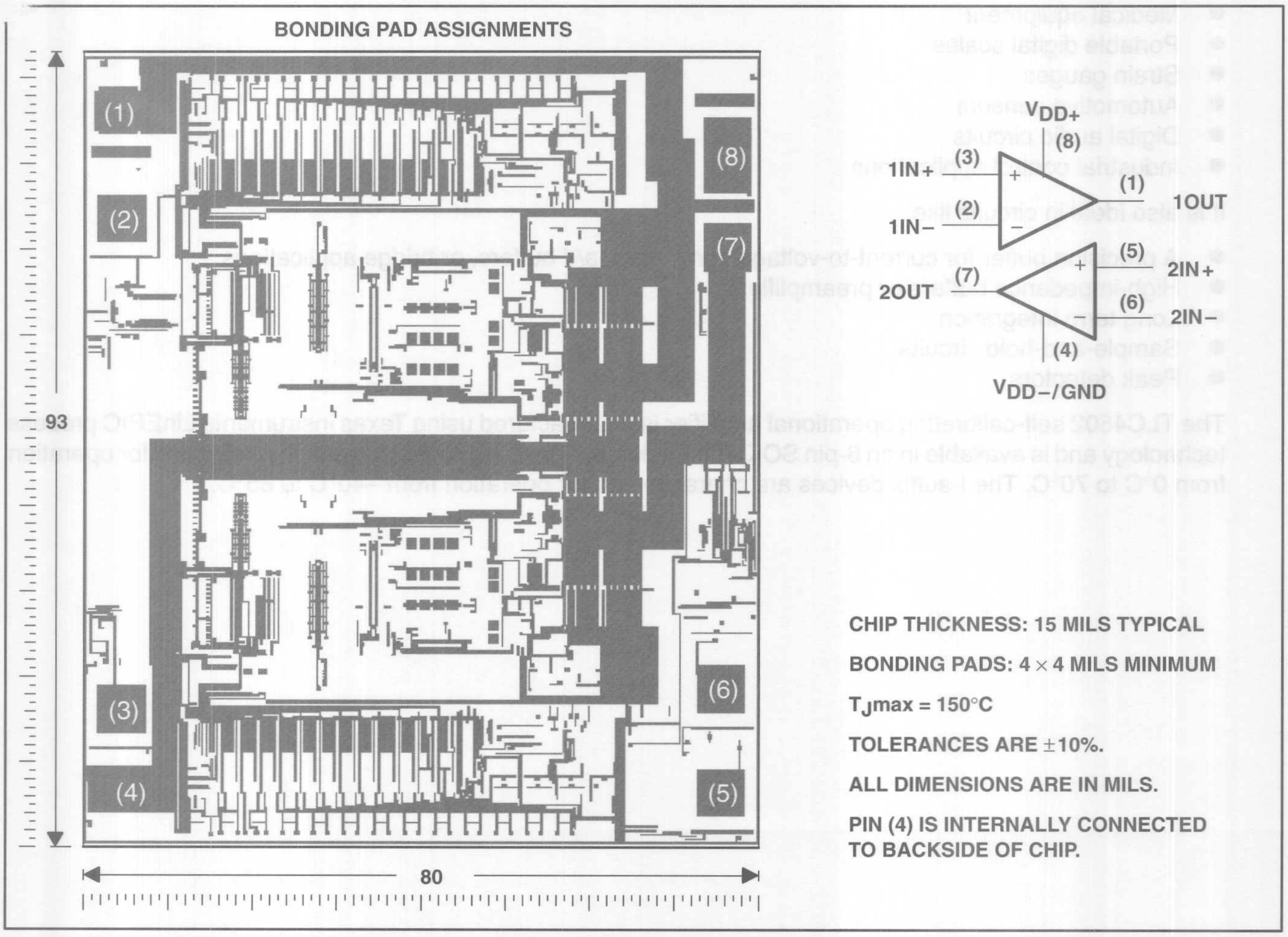
- A precision buffer for current-to-voltage converters, a/d buffers, or bridge applications
- High-impedance buffers or preamplifiers
- Long term integration
- Sample-and-hold circuits
- Peak detectors

The TLC4502 self-calibrating operational amplifier is manufactured using Texas instruments LinEPIC process technology and is available in an 8-pin SOIC (D) Package. The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C.

chip information

chip, when properly assembled, display characteristics similar to the TLC4502C. Thermal compression ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip can be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD+} (see Note 1)	7 V
Differential input voltage, V_{ID} (see Note 2)	±7 V
Input voltage range, V_I (any input, see Note 1)	−0.3 V to 7 V
Input current, I_I (each input)	±5 mA
Output current, I_O (each output)	±100 mA
Total current into V_{DD+}	±100 mA
Total current out of V_{DD-}/GND	±100 mA
Electrostatic discharge (ESD)	> 2 kV
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: TLC4502C	0°C to 70°C
TLC4502I	−40°C to 85°C
Storage temperature range, T_{stg}	−65°C to 150°C
Case temperature for 60 seconds, T_C: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to V_{DD-}/GND.
2. Differential voltages are at IN+ with respect to IN−. Excessive current flows when an input is brought below $V_{DD-} - 0.3$ V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW

recommended operating conditions

	TLC4502C		TLC4502I		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}	4	6	4	6	V
Input voltage range, V_I	V_{DD-}	$V_{DD+} - 2.3$	V_{DD-}	$V_{DD+} - 2.3$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 2.3$	V_{DD-}	$V_{DD+} - 2.3$	V
Operating free-air temperature, T_A	0	70	−40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, GND = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC4502C			TLC4502AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD} = \pm 2.5$ V, $V_{IC} = 0$,	$V_O = 0$, $R_S = 50\ \Omega$	25°C	–100		100	–50		50	μV
				Full range	–100		100	–50		50	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		1			1		μV/°C
I_{IO}	Input offset current			25°C		1			1		pA
				Full range			500			500	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			500			500	
V_{OH}	High-level output voltage	$I_{OH} = -500\ \mu A$		25°C		4.99			4.99		V
		$I_{OH} = -5$ mA		25°C		4.9			4.9		
				Full range	4.7			4.7			
V_{OL}	Low-level output voltage	$V_{IC} = 2.5$ V,	$I_{OL} = 500\ \mu A$	25°C		0.01			0.01		V
		$V_{IC} = 2.5$ V,	$I_{OL} = 5$ mA	25°C		0.1			0.1		
				Full range			0.3			0.3	
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5$ V, $R_L = 1\ k\Omega$,	$V_O = 1$ V to 4 V, See Note 4	25°C	200	1000		200	1000		V/mV
				Full range	200			200			
$R_{I(D)}$	Differential input resistance			25°C		10			10		kΩ
R_L	Input resistance	See Note 4		25°C		10^{12}			10^{12}		Ω
C_L	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_O	Closed-loop output impedance	$A_V = 10$,	f = 100 kHz	25°C		1			1		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 2.7 V, $V_O = 2.5$ V, $R_S = 1\ k\Omega$		25°C	90	100		90	100		dB
				Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD} = 4$ V to 6 V, $V_{IC} = 0$, No load		25°C	90	100		90	100		dB
				Full range	90			90			
I_{DD}	Supply current	$V_O = 2.5$ V,	No load	25°C		2.5	3.5		2.5	3.5	mA
				Full range			4			4	
$V_{IT(CAL)}$	Calibration input threshold voltage			Full range	4			4			V

† Full range is 0°C to 70°C.

NOTE 4: R_L and C_L values are referenced to 2.5 V.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, GND = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC4502I			TLC4502AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{DD} = ±2.5 V, V_O = 0, V_{IC} = 0, R_S = 50 Ω	25°C	−100		100	−50		50	µV
			Full range	−100		100	−50		50	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1			1		µV/°C
I_{IO}	Input offset current		25°C		1			1		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			500			500	
V_{OH}	High-level output voltage	I_{OH} = – 500 µA	25°C		4.99			4.99		V
		I_{OH} = – 5 mA	25°C		4.9			4.9		
			Full range	4.7			4.7			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 500 µA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V, I_{OL} = 5 mA	25°C		0.1			0.1		
			Full range			0.3			0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 1 kΩ, See Note 4	25°C	200	1000		200	1000		V/mV
			Full range	200			200			
$R_{I(D)}$	Differential input resistance		25°C		10			10		kΩ
R_L	Input resistance	See Note 4	25°C		10^{12}			10^{12}		Ω
C_L	Common-mode input capacitance	f = 10 kHz, P package	25°C		8			8		pF
z_O	Closed-loop output impedance	A_V = 10, f = 100 kHz	25°C		1			1		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 1 kΩ	25°C	90	100		90	100		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4 V to 6 V, V_{IC} = 0, No load	25°C	90	100		90	100		dB
			Full range	90			90			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		2.5	3.5		2.5	3.5	mA
			Full range			4			4	
$V_{IT(CAL)}$	Calibration input threshold voltage		Full range	4			4			V

† Full range is –40°C to 85°C.

NOTE 4: R_L and C_L values are referenced to 2.5 V.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC4502C, TLC4502AC MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V,	C_L = 100 pF	25°C	1.5	2.5		V/µs
				Full range	1			V/µs
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		70		nV/√Hz
		f = 1 kHz		25°C		12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		25°C		1		µV
		f = 0.1 to 10 Hz		25°C		1.5		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 10 kHz, R_L = 1 kΩ, C_L = 100 pF	A_V = 1	25°C		0.02%		
			A_V = 10	25°C		0.08%		
			A_V = 100	25°C		0.55%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 1 kΩ,	25°C		4.7		MHz
B_{OM}	Maximum output swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 1 kΩ,	A_V = 1, C_L = 100 pF	25°C		1		MHz
t_s	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 1 kΩ, C_L = 100 pF	to 0.1%	25°C		1.6		µs
			to 0.01%	25°C		2.2		
ϕ_m	Phase margin at unity gain	R_L = 1 kΩ,	C_L = 100 pF	25°C		74		
	Calibration time			25°C		300		ms

† Full range is 0°C to 70°C.

NOTE 4: R_L and C_L values are referenced to 2.5 V.

operating characteristics, V_{DD} = 5 V

	PARAMETER	TEST CONDITIONS		T_A†	TLC4502I, TLC4502AI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V,	C_L = 100 pF	25°C	1.5	2.5		V/µs
				Full range	1			V/µs
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		70		nV/√Hz
		f = 1 kHz		25°C		12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		25°C		1		µV
		f = 0.1 to 10 Hz		25°C		1.5		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 10 kHz, R_L = 1 kΩ, C_L = 100 pF	A_V = 1	25°C		0.02%		
			A_V = 10	25°C		0.08%		
			A_V = 100	25°C		0.55%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 1 kΩ,	25°C		4.7		MHz
B_{OM}	Maximum output swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 1 kΩ,	A_V = 1, C_L = 100 pF	25°C		1		MHz
t_s	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 1 kΩ, C_L = 100 pF	to 0.1%	25°C		1.6		µs
			to 0.01%	25°C		2.2		
ϕ_m	Phase margin at unity gain	R_L = 1 kΩ,	C_L = 100 pF	25°C		74		
	Calibration time			25°C		300		ms

† Full range is −40°C to 85°C.
NOTE 4: R_L and C_L values are referenced to 2.5 V.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, GND = 0, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC4502Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{DD} = ±2.5 V, V_{IC} = 0,	V_O = 0, R_S = 50 Ω		10		µV
I_{IO}	Input offset current				1		pA
I_{IB}	Input bias current				1		pA
V_{OH}	High-level output voltage	I_{OH} = – 500 µA			4.99		V
		I_{OH} = – 5 mA			4.9		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 500 µA		0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 5 mA		0.1		
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, R_L = 1 kΩ,	V_O = 1 V to 4 V, See Note 4		1000		V/mV
$R_{I(D)}$	Differential input resistance				10		kΩ
R_L	Input resistance	See Note 4			10^{12}		Ω
C_L	Common-mode input capacitance	f = 10 kHz,	P package		8		pF
z_O	Closed-loop output impedance	A_V = 10,	f = 100 kHz		1		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, R_S = 1 kΩ	V_O = 2.5 V,		100		dB
k_{SVR}	Supply-voltage rejection ratio $(\Delta V_{DD} \pm/\Delta V_{IO})$	V_{DD} = ±2 V to ±3 V, No load	V_{IC} = 0,		100		dB
I_{DD}	Supply current	V_O = 2.5 V,	No load		2.5		mA

NOTE 4: R_L and C_L values are referenced to 2.5 V.

operating characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLC4502Y			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V,	C_L = 100 pF		2.5		V/µs
V_n	Equivalent input noise voltage	f = 10 Hz			70		nV/√Hz
		f = 1 kHz			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz			1		µV
		f = 0.1 to 10 Hz			1.5		
I_n	Equivalent input noise current				0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 10 kHz, R_L = 1 kΩ, C_L = 100 pF	A_V = 1		0.02%		
			A_V = 10		0.08%		
			A_V = 100		0.55%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 1 kΩ,		4.7		MHz
B_{OM}	Maximum output swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 1 kΩ,	A_V = 1, C_L = 100 pF		1		MHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 1 kΩ, C_L = 100 pF	to 0.1%		1.6		µs
			to 0.01%		2.2		
ϕ_m	Phase margin at unity gain	R_L = 1 kΩ,	C_L = 100 pF		74		
	Calibration time				300		ms

NOTE 4: R_L and C_L values are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1, 2, 3
		vs Common-mode input voltage	4
α_{VIO}	Input offset voltage temperature coefficient	Distribution	5, 6
V_{OH}	High-level output voltage	vs High-level output current	7
V_{OL}	Low-level output voltage	vs Low-level output current	8
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	9
I_{OS}	Short-circuit output current	vs Free-air temperature	10
V_O	Output voltage	vs Differential input voltage	11
A_{VD}	Large-signal differential voltage amplification	vs Free-air temperature vs Frequency	12 13
z_o	Output impedance	vs Frequency	14
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	15 16
SR	Slew rate	vs Load capacitance vs Free-air temperature	17 18
	Inverting large-signal pulse response	vs Time	19
	Voltage-follower large-signal pulse response	vs Time	20
	Inverting small-signal pulse response	vs Time	21
	Voltage-follower small-signal pulse response	vs Time	22
V_n	Equivalent input noise voltage	vs Frequency	23
	Input noise voltage	Over a 10-second period	24
THD + N	Total harmonic distortion plus noise	vs Frequency	25
	Gain-bandwidth product	vs Free-air temperature	26
ϕ_m	Phase margin	vs Load capacitance	27, 28
		vs Frequency	13
PSRR	Power-supply rejection ratio	vs Free-air temperature	29
	Calibration time at –40°C	vs Time	30
	Calibration time at 25°C	vs Time	31
	Calibration time at 85°C	vs Time	32

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC4502 INPUT OFFSET VOLTAGE

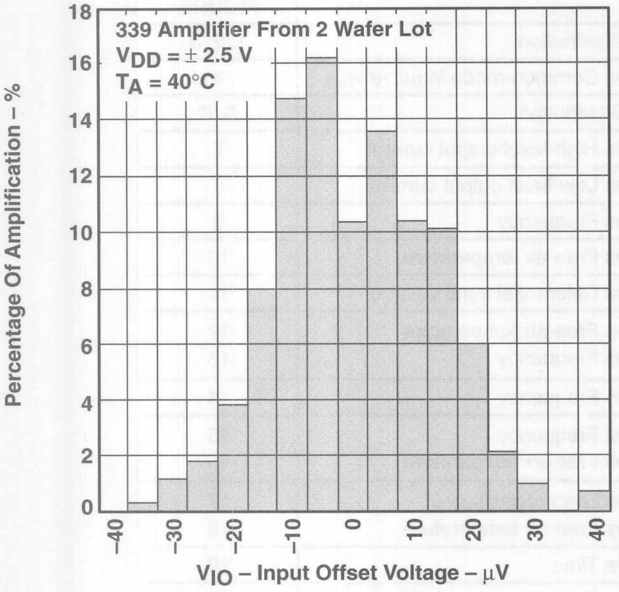


Figure 1

DISTRIBUTION OF TLC4502 INPUT OFFSET VOLTAGE

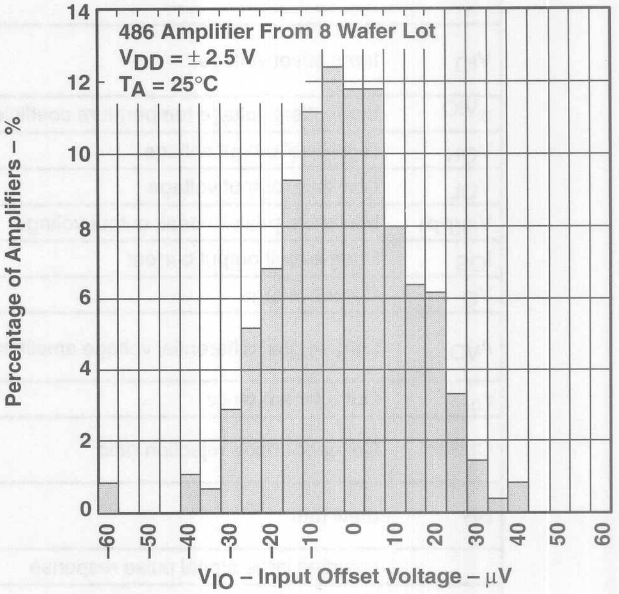


Figure 2

DISTRIBUTION OF TLC4502 INPUT OFFSET VOLTAGE

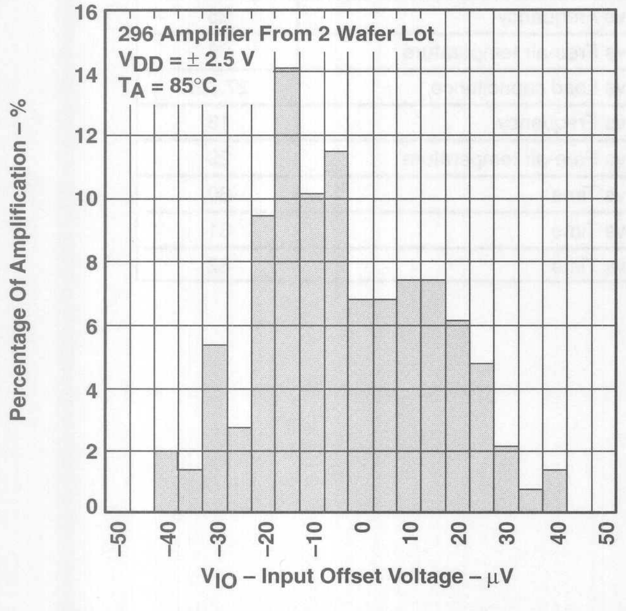


Figure 3

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

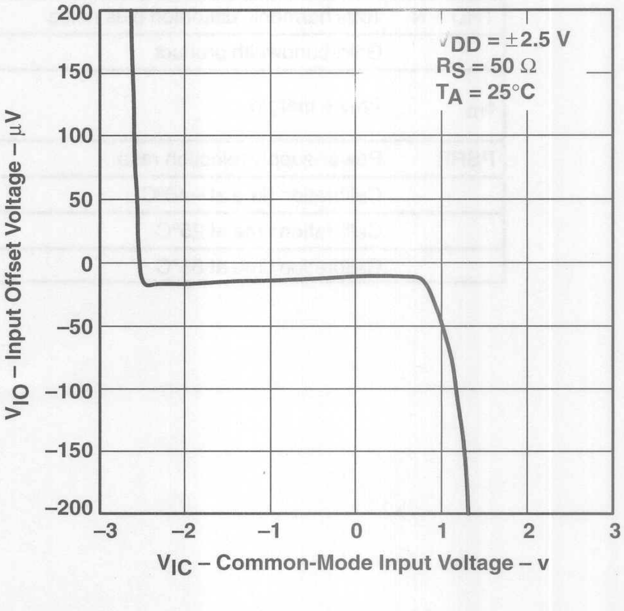
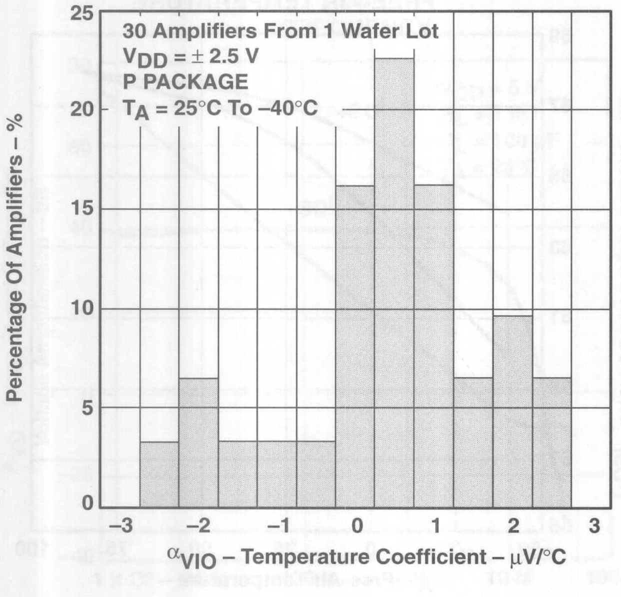


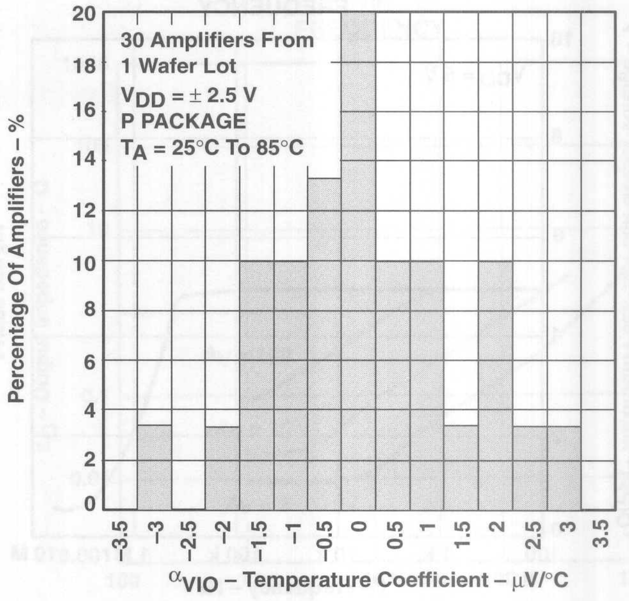
Figure 4

TYPICAL CHARACTERISTICS



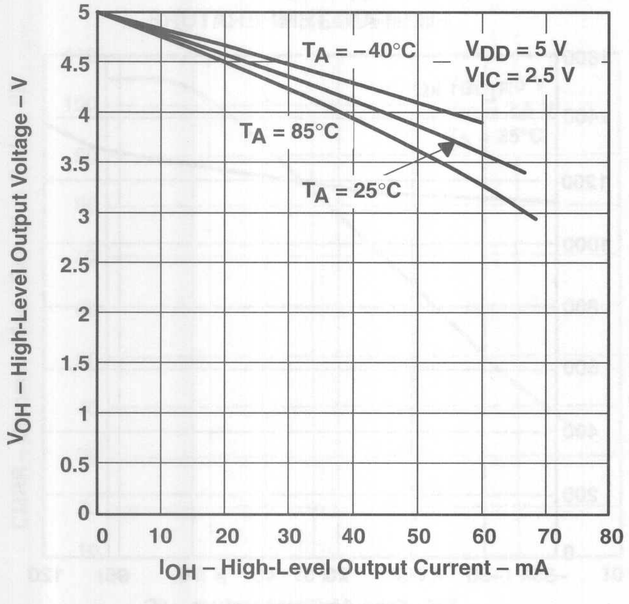
DISTRIBUTION OF TLC4502 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

Figure 5



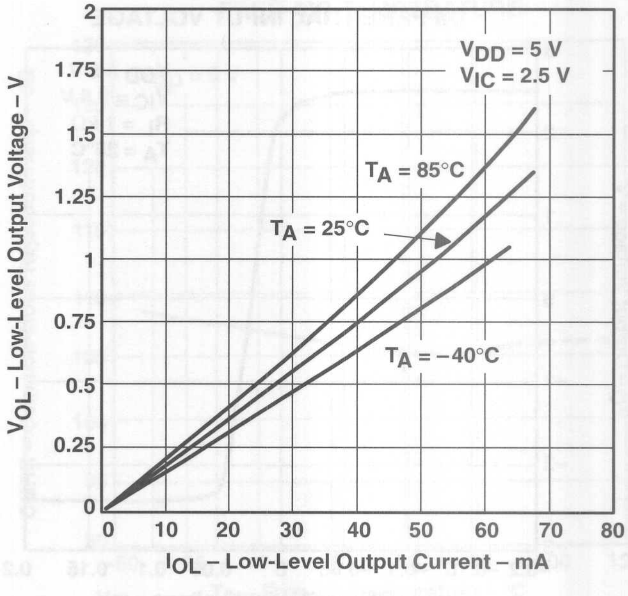
DISTRIBUTION OF TLC4502 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

Figure 6



HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 7



LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

Figure 8

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

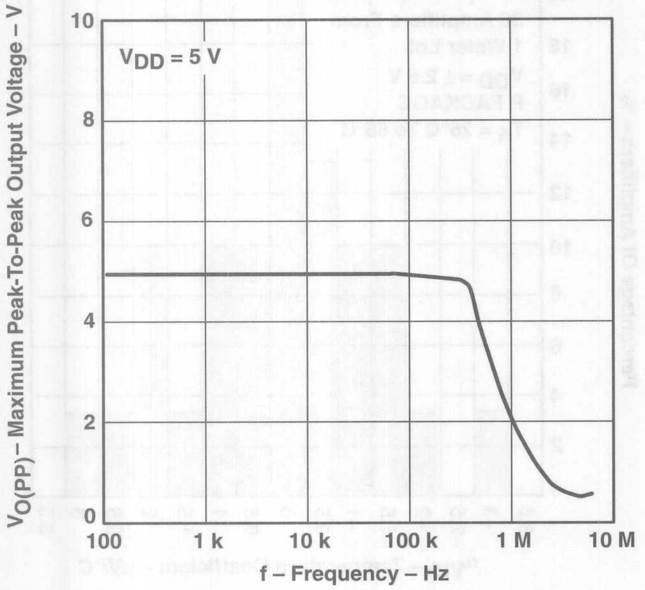


Figure 9

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

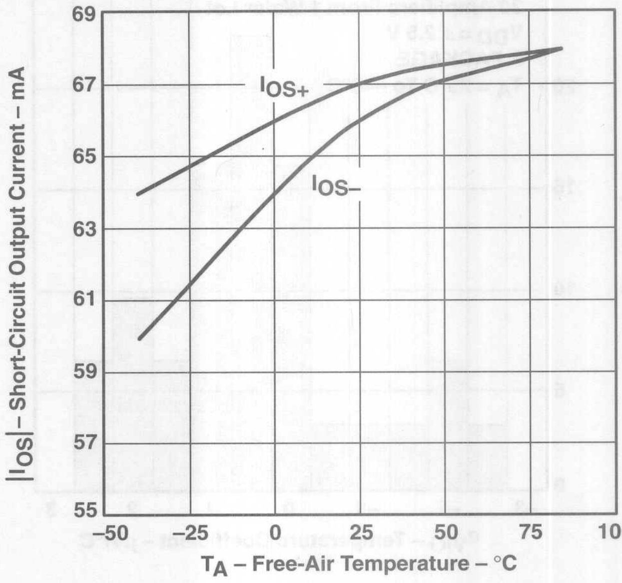


Figure 10

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

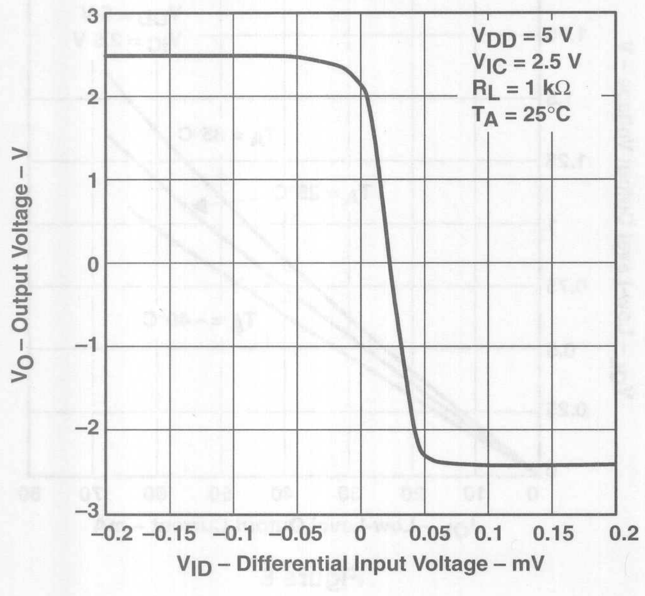


Figure 11

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

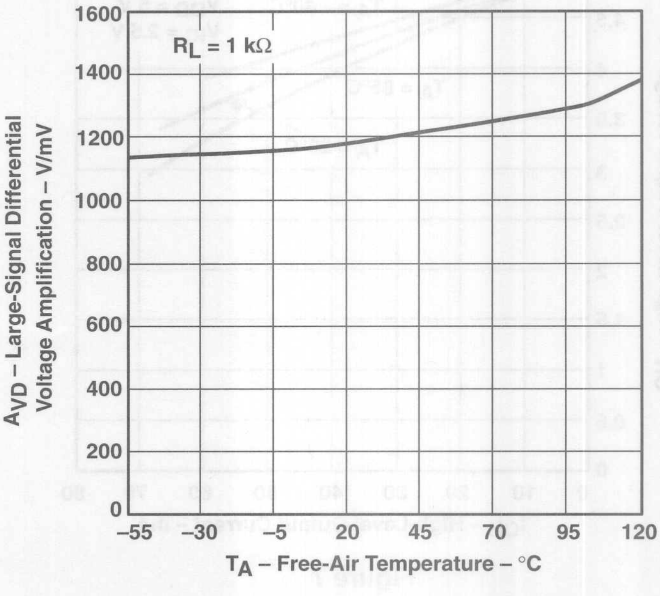


Figure 12

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

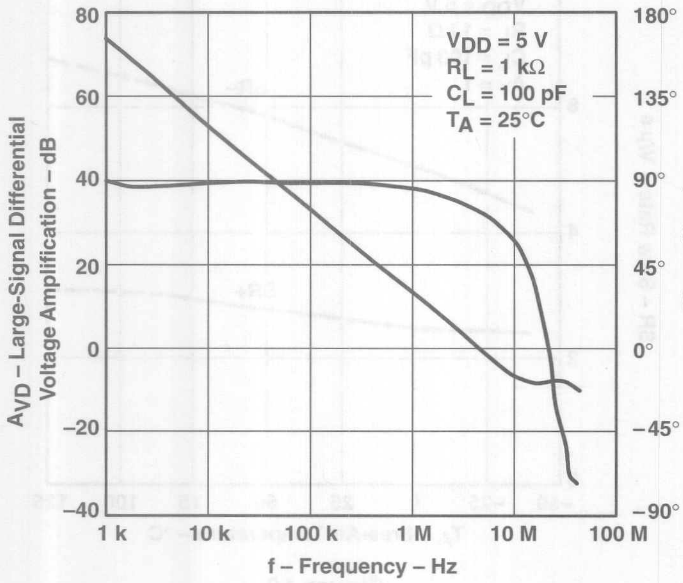


Figure 13

OUTPUT IMPEDANCE vs FREQUENCY

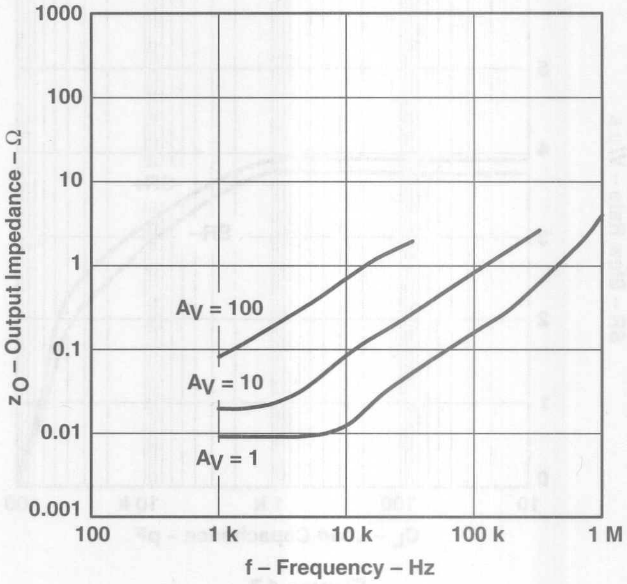


Figure 14

COMMON-MODE REJECTION RATIO vs FREQUENCY

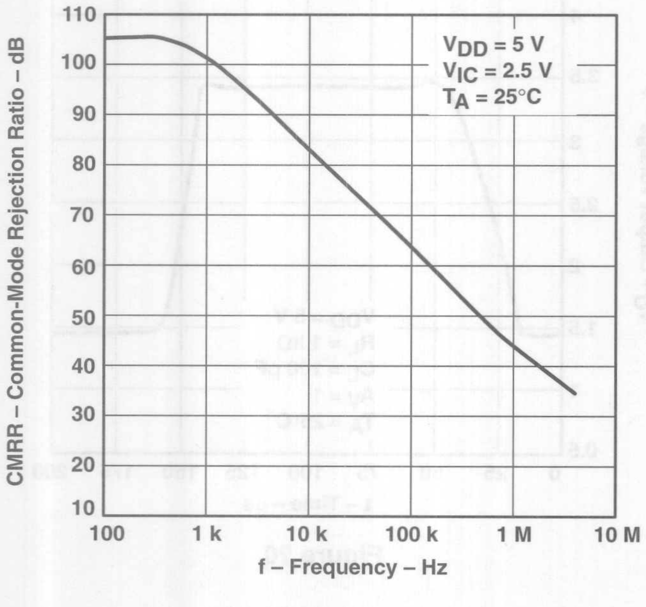


Figure 15

COMMON-MODE REJECTION RATIO vs FREQUENCY

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

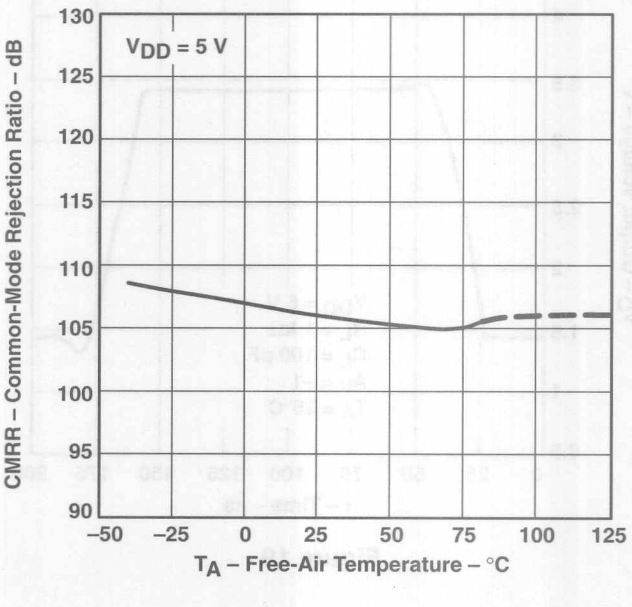


Figure 16

TYPICAL CHARACTERISTICS

SLEW RATE vs LOAD CAPACITANCE

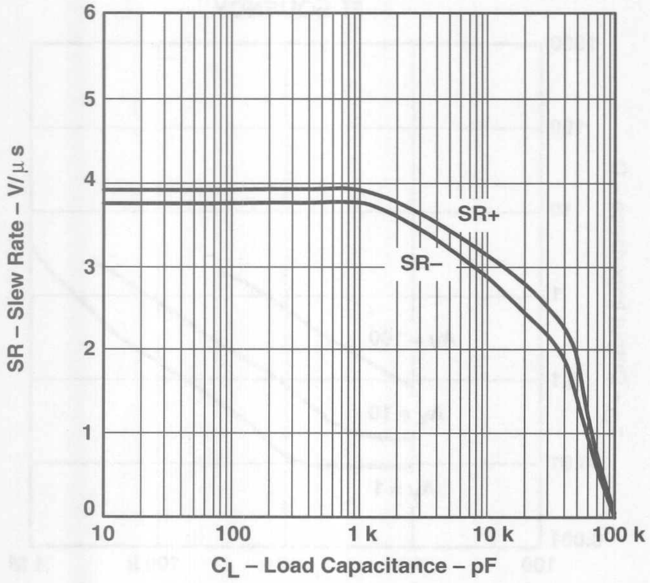


Figure 17

SLEW RATE vs FREE-AIR TEMPERATURE

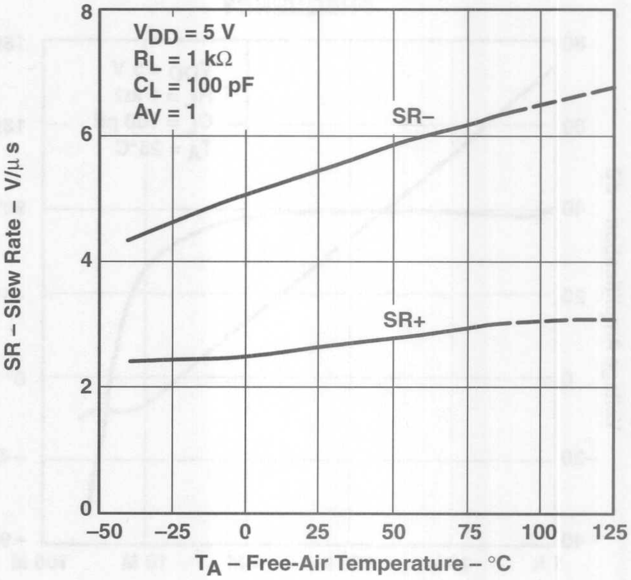


Figure 18

INVERTING LARGE-SIGNAL PULSE RESPONSE

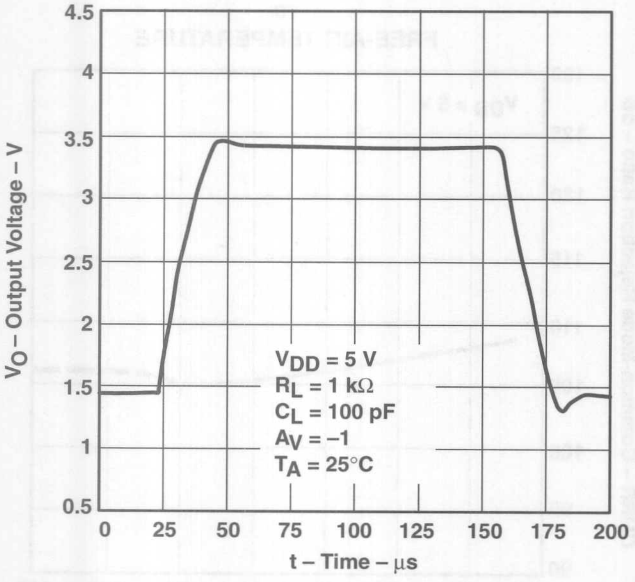


Figure 19

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

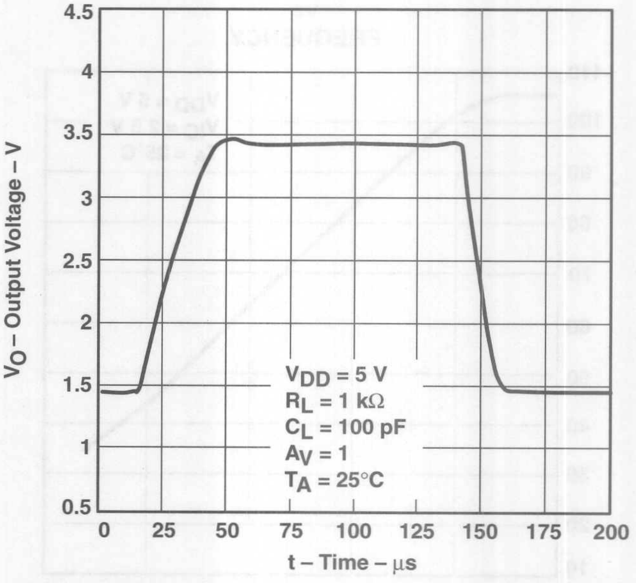


Figure 20

TYPICAL CHARACTERISTICS

INVERTING SMALL-SIGNAL PULSE RESPONSE

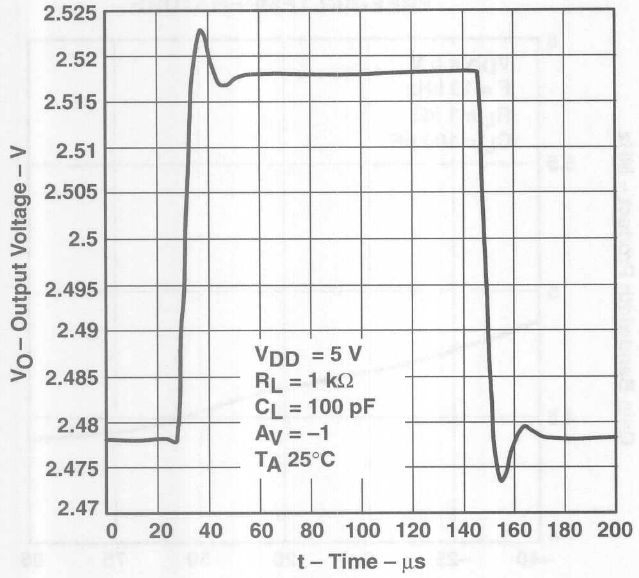


Figure 21

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

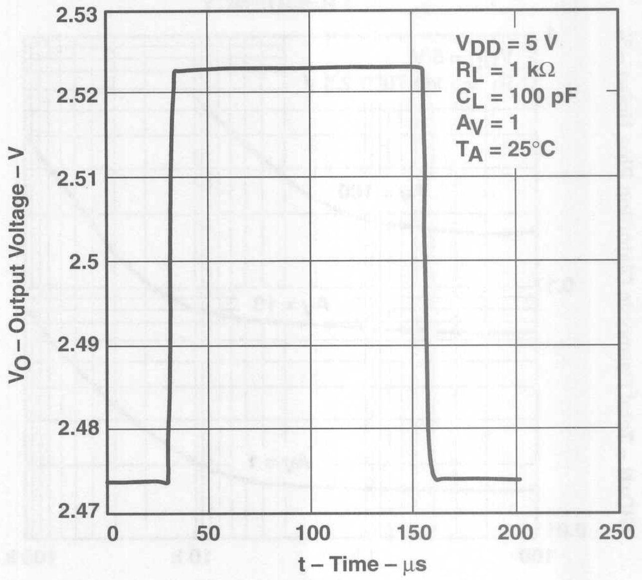


Figure 22

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

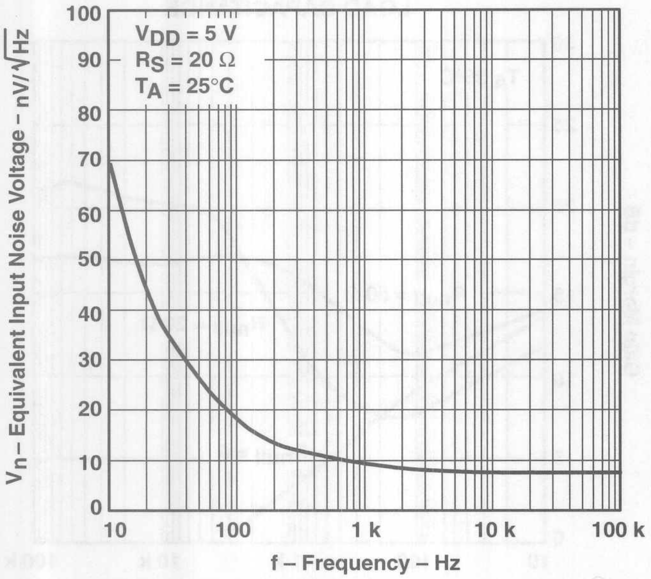


Figure 23

INPUT NOISE VOLTAGE OVER
A 10-SECOND PERIOD

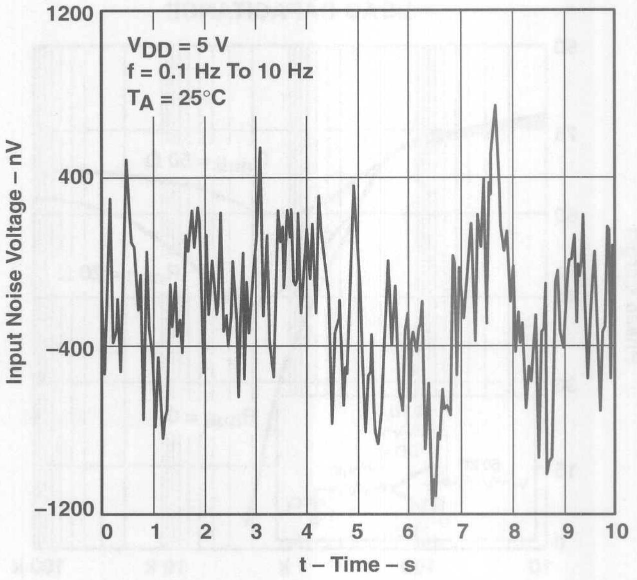


Figure 24

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

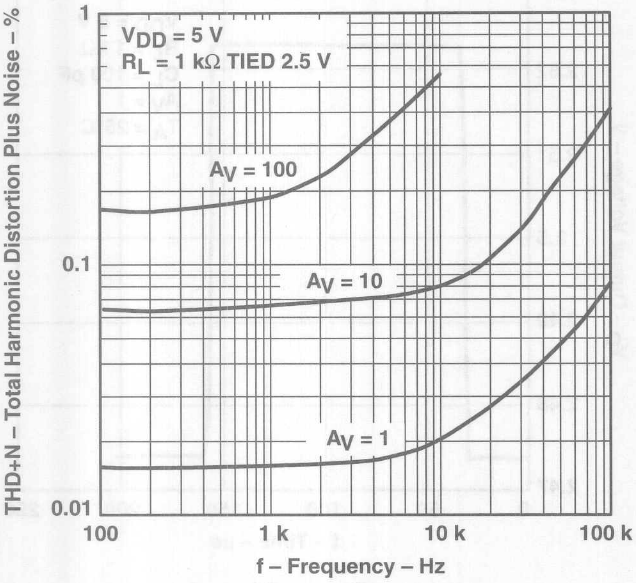


Figure 25

GAIN-BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE

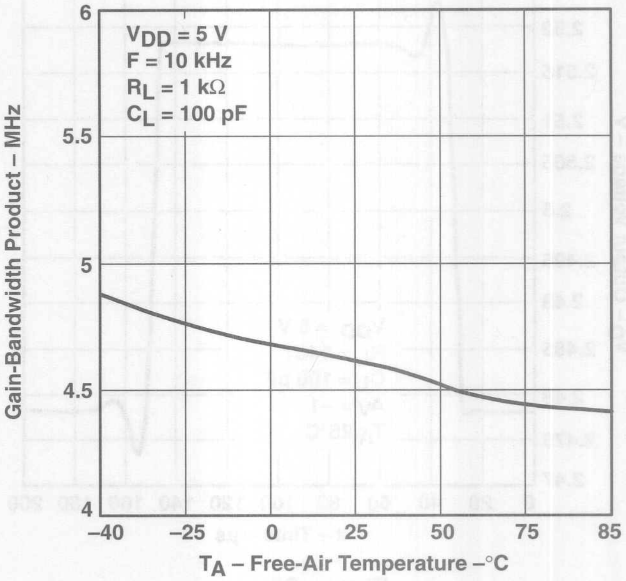


Figure 26

PHASE MARGIN vs LOAD CAPACITANCE

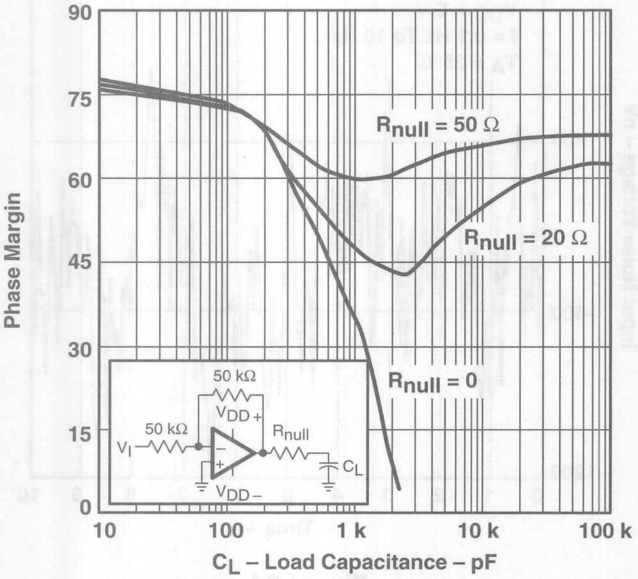


Figure 27

GAIN MARGIN vs LOAD CAPACITANCE

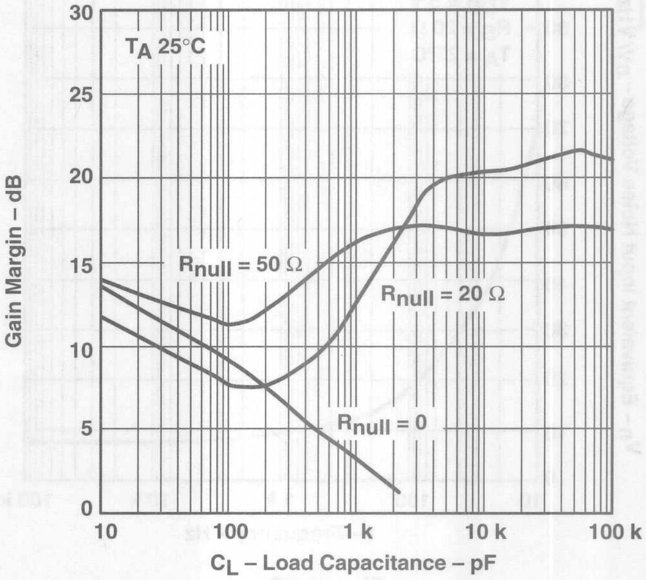


Figure 28

TYPICAL CHARACTERISTICS

POWER SUPPLY REJECTION RATIO
vs
FREE-AIR TEMPERATURE

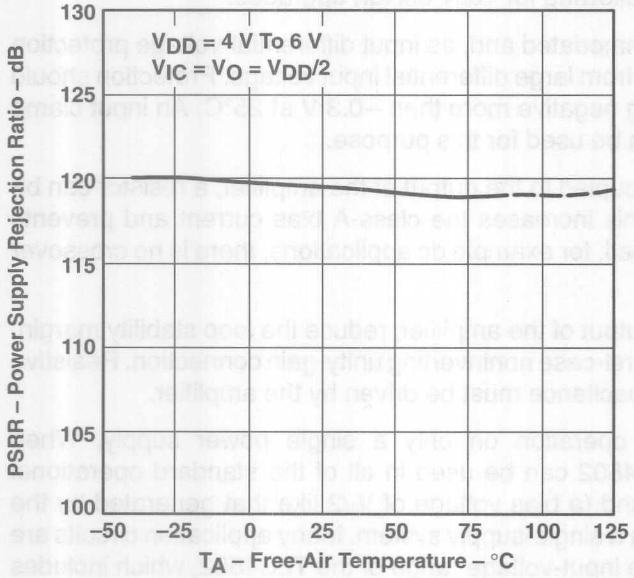


Figure 29

CALIBRATION TIME AT –40°C

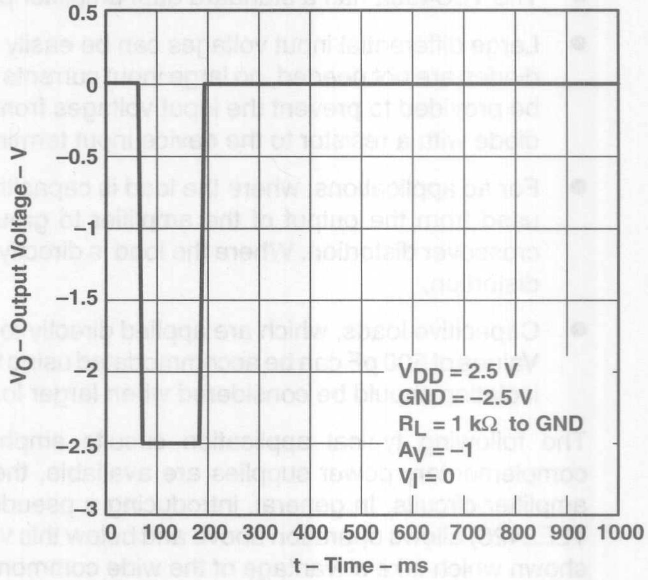


Figure 30

CALIBRATION TIME AT 25°C

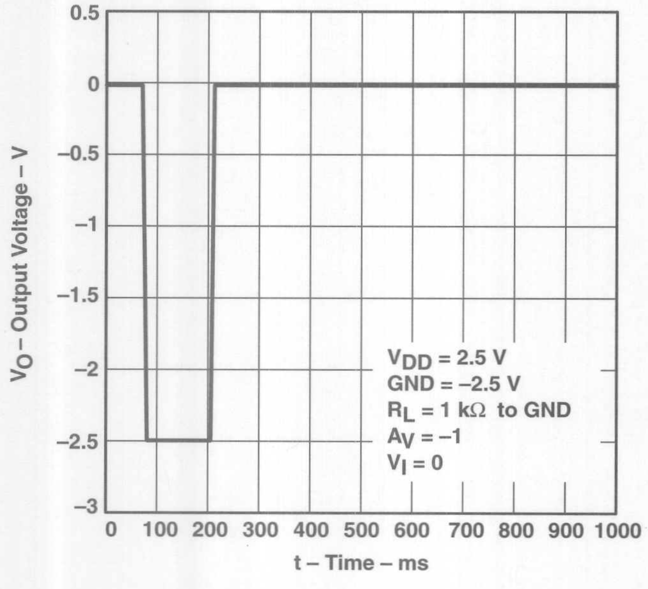


Figure 31

CALIBRATION TIME AT 85°C

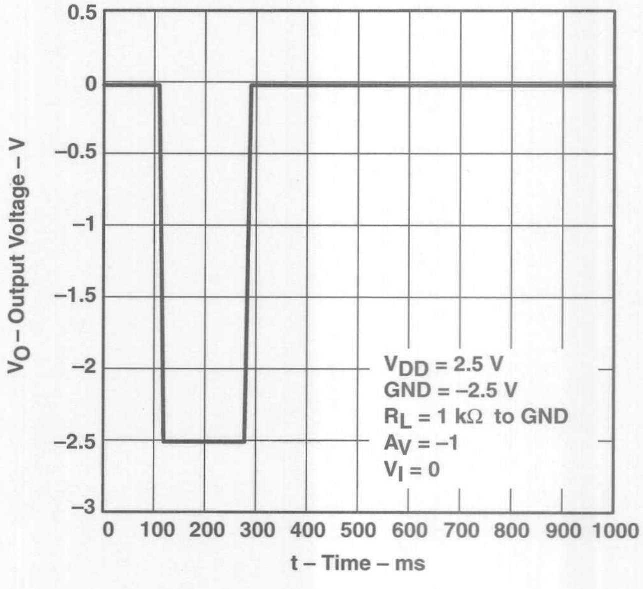


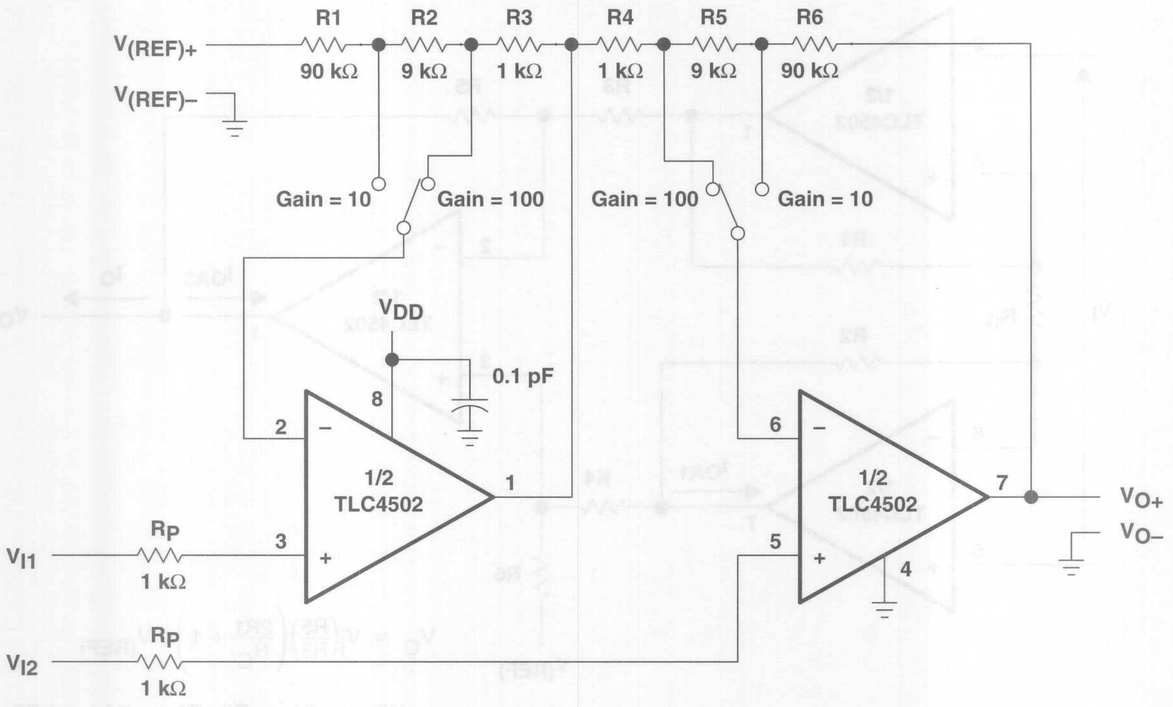
Figure 32

APPLICATION INFORMATION

- The TLC4502 is designed to operate with only a single 5-V power supply, have true differential inputs, and remain in the linear mode with an input common-mode voltage of 0.
- The TLC4502 has a standard dual-amplifier pinout allowing for easy design upgrades.
- Large differential input voltages can be easily accommodated and, as input differential-voltage protection diodes are not needed, no large input currents result from large differential input voltage. Protection should be provided to prevent the input voltages from going negative more than −0.3 V at 25°C. An input clamp diode with a resistor to the device input terminal can be used for this purpose.
- For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor can be used from the output of the amplifier to ground. This increases the class-A bias current and prevents crossover distortion. Where the load is directly coupled, for example dc applications, there is no crossover distortion.
- Capacitive loads, which are applied directly to the output of the amplifier, reduce the loop stability margin. Values of 500 pF can be accommodated using the worst-case noninverting unity-gain connection. Resistive isolation should be considered when larger load capacitance must be driven by the amplifier.

The following typical application circuits emphasize operation on only a single power supply. When complementary power supplies are available, the TLC4502 can be used in all of the standard operational amplifier circuits. In general, introducing a pseudo-ground (a bias voltage of $V_I/2$ like that generated by the TLE2426) allows operation above and below this value in a single-supply system. Many application circuits are shown which take advantage of the wide common-mode input-voltage range of the TLC4502, which includes ground. In most cases, input biasing is not required and input voltages that range to ground can easily be accommodated.

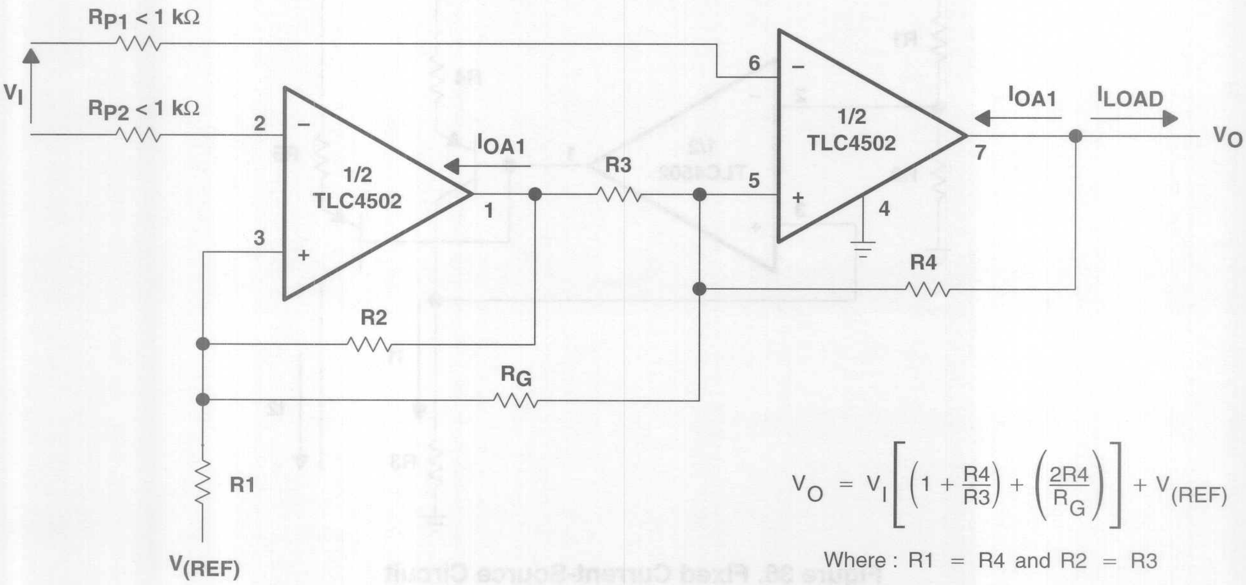
APPLICATION INFORMATION



$$(\text{Gain} = 10)\quad V_O = \left(V_{I1}\ V_{I2}\right)\left(1 + \frac{R6}{R4 + R5}\right) + V_{(REF)}\quad \text{Where } R1 = R6,\ R2 = R5,\ \text{and } R3 = R4$$

$$(\text{Gain} = 100)\quad V_O = \left(V_{I1} - V_{I2}\right)\left(1 + \frac{R5 + R6}{R4}\right) + V_{(REF)}\quad \text{Where } R1 = R6,\ R2 = R5,\ \text{and } R3 = R4$$

Figure 33. Single-Supply Programmable Instrumentation Amplifier Circuit

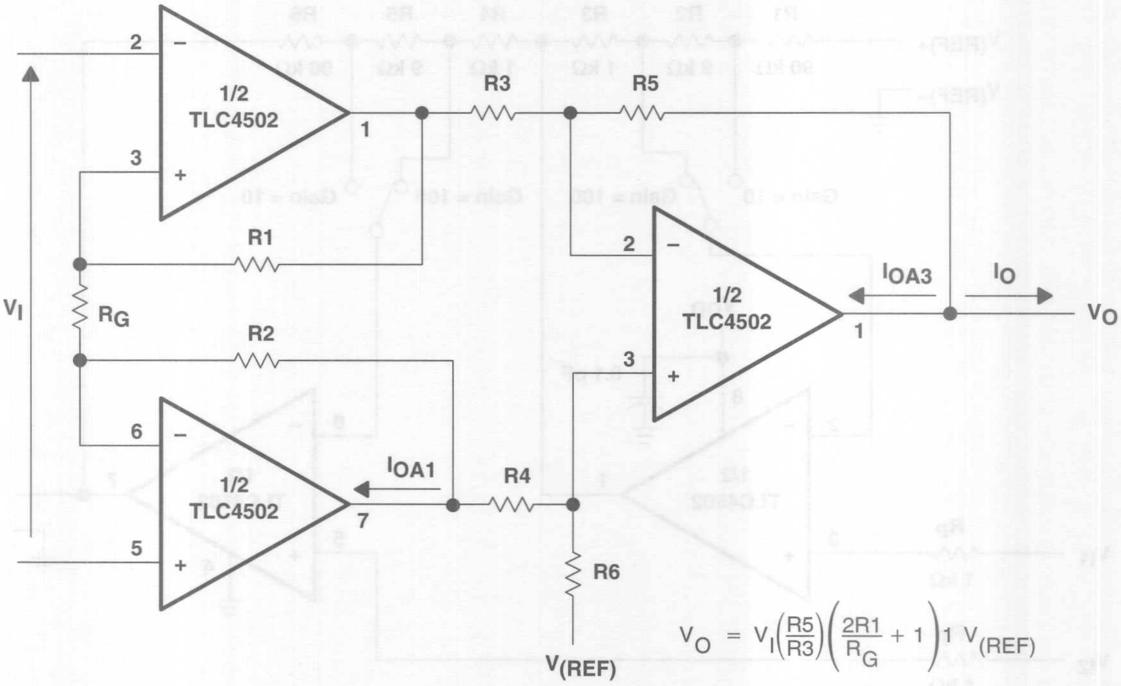


$$V_O = V_I\left[\left(1 + \frac{R4}{R3}\right) + \left(\frac{2R4}{R_G}\right)\right] + V_{(REF)}$$

Where : R1 = R4 and R2 = R3

Figure 34. Two Operational-Amplifier Instrumentation Amplifier Circuit

APPLICATION INFORMATION



$$V_O = V_I\left(\frac{R5}{R3}\right)\left(\frac{2R1}{R_G} + 1\right)1\ V_{(REF)}$$

Where : R1 = R2, R3 = R4, and R5 = R6

Figure 35. Three Operational-Amplifier Instrumentation Amplifier Circuit

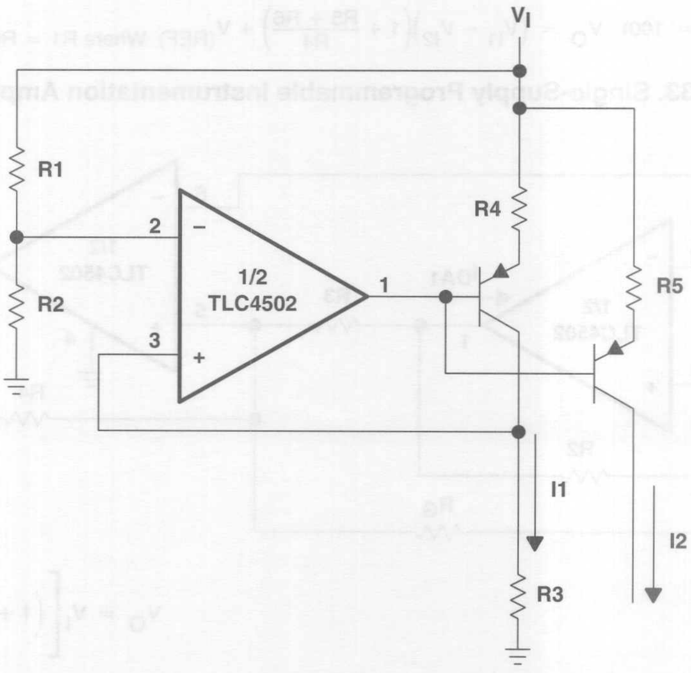


Figure 36. Fixed Current-Source Circuit

APPLICATION INFORMATION

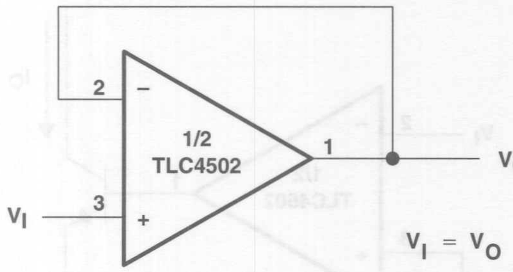


Figure 37. Voltage-Follower Circuit

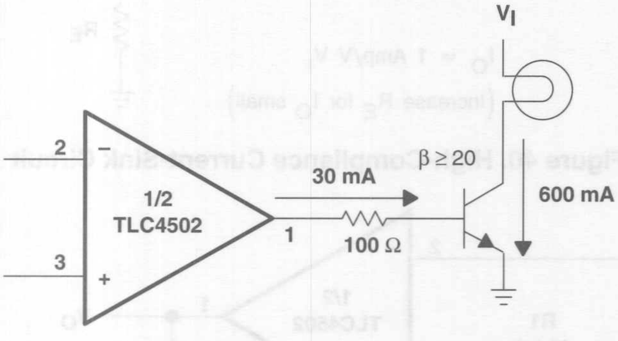


Figure 38. Lamp-Driver Circuit

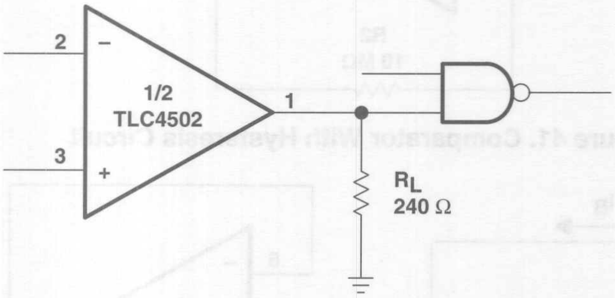


Figure 39. TTL-Driver Circuit

APPLICATION INFORMATION

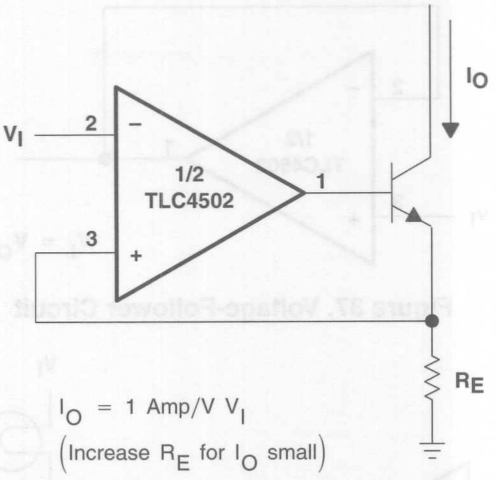


Figure 40. High-Compliance Current-Sink Circuit

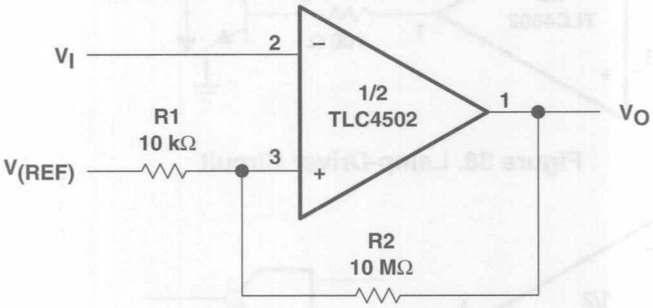


Figure 41. Comparator With Hysteresis Circuit

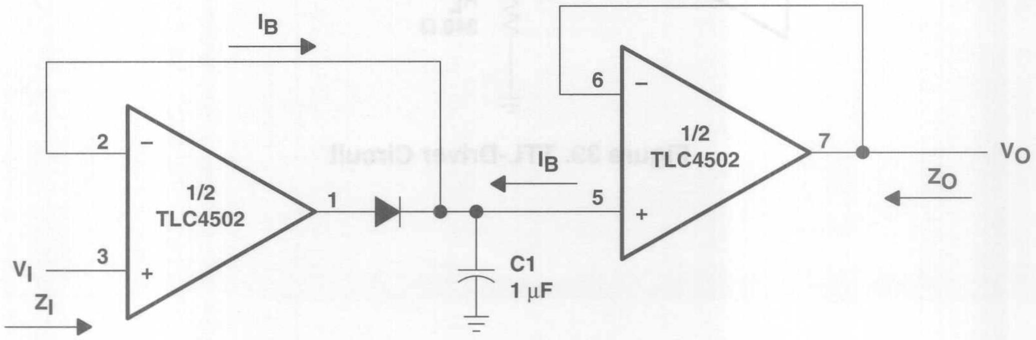
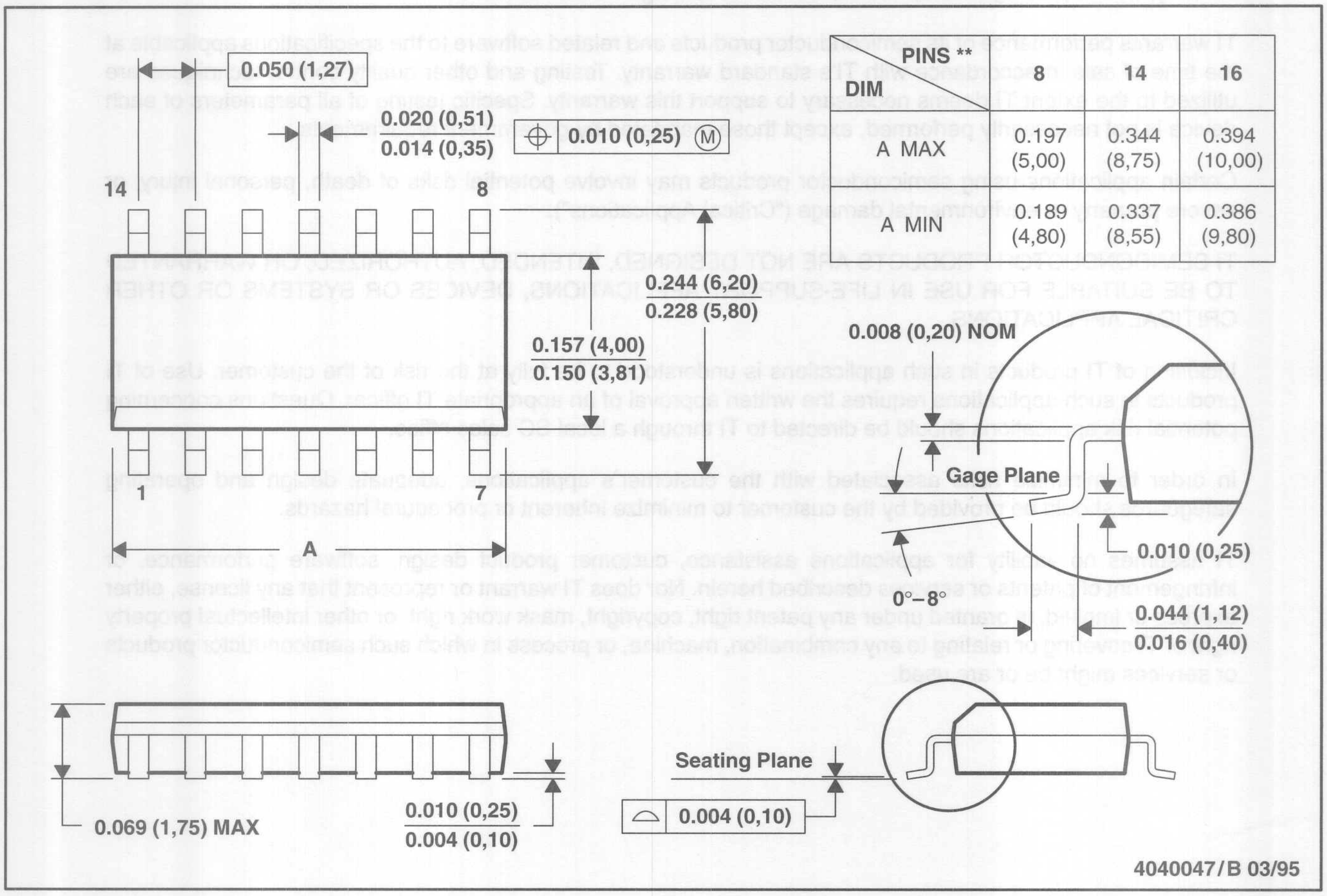


Figure 42. Low-Drift Detector Circuit

MECHANICAL INFORMATION

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
- D. Four center pins are connected to die mount pad.
- E. Falls within JEDEC MS-012

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